

REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 1, 3, 6 and 7 have been amended. Claims 11-29 have been previously withdrawn. Thus, claims 1-10 are currently pending in the application and subject to examination.

In the Office Action mailed June 13, 2006, claim 3 was rejected under 35 U.S.C. § 112, second paragraph. Claim 3 has been amended responsive to this rejection. If any additional amendment is necessary to overcome this rejection, the Examiner is requested to contact the Applicant's undersigned representative.

In the outstanding Office Action, claims 1-10 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,757,763 to Preiss et al. (hereinafter "Preiss"). It is noted that claims 1, 3, 6 and 7 have been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicant hereby traverses the rejection, as follows.

The Applicant's invention is directed to an inter-bus communication interface device for controlling data communication between a first bus and a second bus. In the Applicant's invention as recited in amended claim 1, a buffer is provided for storing only communication data sent from a first device connected to a first bus, a register is provided for storing only communication control information concerning the communication data, and a control circuit is provided for passing the communication data stored in the buffer to a second device connected to a second bus, and for passing the communication control information stored in the register to the second device.

Thus, in the Applicant's claimed invention, data is transmitted via a buffer and communication control information to be referenced in data processing is transmitted via a register.

Moreover, in the Applicant's claimed invention, the communication control information is equivalent to control information that is set in a general communication packet. That is, before the data of the buffer is all read out, control information can be acquired and an appropriate process can be performed according to the control information. Thus, the communication control information is information that is used for directing a CPU's communication processing, and is written in by software. This configuration can eliminate the need of conventional operations where, before an appropriate process is performed, the data of a buffer is all read out and control information set together with the data in the buffer is then extracted.

Preiss, however, teaches a process of transmitting data between different buses via a buffer, in which only information is transmitted via the buffer. More specifically, Preiss teaches a "receive register (806)" and a "transmit register (TXWR register 308)," which are used for a transmission process, as can be seen from Fig. 2B of Preiss. The TXWR register 308 of Preiss includes two byte valid tag bits (BVO and BV1), which are used to indicate valid data bytes in the TXWR register 308, so that when the transfer FIFO state machine (TFWSM 302) receives the synchronized byte valid tag bits, the data in the TXWR register 308 is guaranteed to be stable and is used without further synchronization logic. Thus, it appears the Examiner may be interpreting the byte valid tag bits (BVO, BV1) as communication control information.

However, the byte valid tag bits of Preiss are synchronized to the USBD_CLK and are used as handshake signals by the TFWSM state machine 302 (see, e.g., col. 5, lines 6-17 pf Preiss). Thus, the byte valid tag bits of Preiss are signals used for directly controlling hardware. The "receive register (806)" and "transmit register (TXWR register 308)" of Preiss are not used for transmitting communication control information, as recited in the claimed invention.

In the claimed invention, the contents (data) of a buffer and the contents (communication control information) of a register are transferred in parallel. With this configuration, only contents of the register are transmitted according to necessity. Transmission of communication control information and data via different routes eliminates the necessity for a device receiving the data to extract communication control information by analyzing the data. This realizes more efficient data reception.

Preiss does not disclose such a processing function. For example, according to Preiss, an end packet is identified by detecting Zero data or packet length less than the maximum number (see col. 3, lines 57-58 and col. 4, lines 14-16). Therefore, wasteful data in Preiss is set in the FIFO in order to detect the end packet. On the other hand, according to the claimed invention, a notification of an end point can be made via the register, which can eliminate the need of setting such wasteful data in the buffer.

In addition, Preiss does not teach transmitting the contents of a register to other devices, as recited in the claimed invention.

For at least these reasons, the Applicant submits that claim 1, as amended, is allowable over the applied art of record. As claim 1 is allowable, the Applicant submits

that claims 2-5, which depend from allowable claim 1, are likewise allowable for at least the reasons set forth above with respect to claim 1.

Similarly to as described above with respect to claim 1, the Applicant submits that claim 6 is allowable over the applied art of record, as Preiss neither discloses nor suggests at least the combination of a first buffer for storing only first communication data sent from a first device connected to the first bus; a first register for storing only first communication control information concerning the first communication data; a second buffer for storing only second communication data sent from a second device connected to the second bus; a second register for storing only second communication control information concerning the second communication data; and a control circuit for passing the first communication data stored in said first buffer to the second device, and the first communication control information stored in said first register to the second device, and further passing the second communication data stored in said second buffer to the first device, and the second communication control information stored in said second register to the first device, as recited in claim 6, as amended.

Similarly to as described above with respect to claims 1 and 6, the Applicant submits that claim 7 is allowable over the applied art of record, as Preiss neither discloses nor suggests at least the combination of an internal CPU; a receive buffer for storing only receive data received from said external host apparatus; a receive register for storing only receive communication control information concerning the receive data; a transmit buffer for storing only transmit data transmitted from said internal CPU via an internal bus; a transmit register for storing only transmit communication control information concerning the transmit data; and a control circuit for passing the receive

data stored in said receive register to said internal CPU and passing the receive communication control information stored in said receive register to said internal CPU, and further passing the transmit data stored in said transmit buffer to said external host apparatus and passing the transmit communication control information stored in said transmit register to said external host apparatus, as recited in claim 7, as amended. As claim 7 is allowable, the Applicant submits that claims 8-10, which depend from allowable claim 7, are likewise allowable for at least the reasons set forth above with respect to claim 7.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 1-10 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this

communication to Deposit Account No. 01-2300 referencing client matter number
107337-00106.

Respectfully submitted,

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Enclosures: Petition for Extension of Time (two months)